REMARKS

Claims 1, 3, 6, 8, 22, and 33 are amended, claim 2 is canceled, and no claims are added; as a result, claims 1 and 3-37 are now pending in this application.

§112 Rejection of the Claims

Claims 1-37 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 2 is canceled, so the rejection of claim 2 is moot. Applicant respectfully requests reconsideration of the rejections of claims 1 and 3-37.

The Office Action on page 2 states, "Re claim 1 limitation 'in parallel' is indefinite in lines 7 and 10 because the second circuit is not operating in parallel with the first circuit as cited in line 7, but rather the second circuit is using the output of the first circuit for operating. Similarly, the sum generator is not operated in parallel with the first circuit and the second circuit as cited in line 10, but rather the sum generator is using the output of the second circuit for selecting final result as seen in Figure 1 of the present invention."

Applicant has removed the limitation "in parallel" in the claims and believes that the rejection under 35 U.S.C. § 112, second paragraph, has been overcome. Applicant respectfully requests withdrawal of the rejection of claims 1-37, and allowance of all claims.

§102 Rejection of the Claims

Claims 1, 7-10, 12, 16, 21-30, 32-34, and 36-37 were rejected under 35 U.S.C. § 102(b) as being anticipated by Goto et al. (U.S. 5,047,976).

Claims 1, 8, 22, and 33 have been amended to includes the additional carry bits limitations from claim 2. Claim 2 which was indicated as allowable by the Examiner if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, second paragraph. Applicant believes they have demonstrated that claims 1-37 are not indefinite, and therefore have overcome the rejection of claims 1-37 under 35 U.S.C. § 112, second paragraph. Thus, claims 1, 8, 22, and 33, and the claims which depend upon claims 1, 8, 22, and 33, now include limitations not found in the Goto et al. patent.

Claims 28-30 Already Distinguishable over Goto et al.

Further, the Goto et al. patent is also distinguishable from the claims since the elements identified by the labels MPX3 and MPX4 in the Goto et al. patent are multiplexers, and are not equivalent to the carry-merge stages claimed by Applicant and defined in the specification of the present patent application. For example, but not by way of limitation, the structure of the adder of the Goto et al. patent is very much different from the claimed structure and methods of the claims as described more fully below.

Applicant's claim 28 recites,

> generating a first predetermined number of carries by merging bits of the two binary numbers to produce a plurality of first carry signals;
> generating a second predetermined number of carries from one of a plurality of stages connected in series by merging bits of previous stages and producing therefrom merged bits for subsequent stages and producing therefrom a plurality of intermediate carry signals. [Emphasis Added].

In contrast, Goto et al. merely discloses partitioned adders 11 and 32-41, wherein at column 9, lines 36-58 Goto et al. states,

> Referring to FIG. 6A, the partitioned adder 12 receives the carry propagate signals P4 through P7 relating to the fourth digit through the seventh digit, the carry generate signals G4 through G7 relating thereto, and the real carry signal C3 supplied from the partitioned adder 11, and then generates the real sum signals F4 through F7, and the provisional carry signals C7(1) and C7(0). The carry propagate signal P4 through P7 are defined by a formula that Pj=Aj[exclusive OR]Bj (j=4 to 7 in this case). The carry generate signals G4 through G7 are defined by a formula such that Gj=Aj·Bj (j=4 to 7 in this case). Signals P4 through P7 are inverted carry propagate signals obtained by inverting the carry propagate signals P4 through P7. Signals G4 through G7 are inverted carry generate signals obtained by inverting the carry generate signals G4 through G7. Signals Cj,1 and Cj,0 are carry signals which are generated by and propagated from a chain of a transfer gate and inverter relating to a digit which is one bit lower than each digit. Signals Cj,1 and Cj,0 are inverted carry signals which are generated by and propagated from a chain of a transfer gate and inverter relating to a digit which is one bit lower than each digit.

Thus, Goto et al. describes carry signals generated by and propagated from a digit which is one bit lower than each digit. However, there is no disclosure in Goto et al. of generating carries by merging bits of the two binary numbers as recited in claim 28. These limitations as recited in claim 28, as well as other not discussed here, are not found in the Goto et al. patent.

Since all of the limitations of claim 28 and the claims which depend upon claim 28 are not found in the single publication by Goto et al., all of the requirements for an anticipation rejection under 35 U.S.C. § 102(b) are not met.

For at least the reasons stated above, Applicant respectfully requests reconsideration of claims 1, 7-10, 12, 16, 21-30, 32-34, and 36-37, and allowance of all claims.

Allowable Subject Matter

Claims 2-6, 11, 13-15, 17-20, 31, and 35 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112 set forth in the Office Action. Applicant has done this and believes claims 3-6, 11, 13-15, 17-20, 31, and 35 are now allowable. Reconsideration of the claims is respectfully solicited.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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